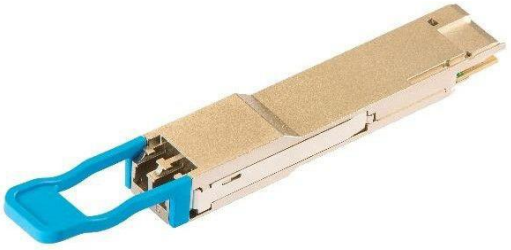
FEATURES



- Hot-pluggable QSFP-DD Type 2 form factor
- Supports 212.5Gb/s aggregate bit rate
- Maximum link length of 10km on Single Mode Fiber (SMF)
- Power dissipation 10.8W
- Case temperature range of 0°Cto+70°C
- Single 3.3V power supply
- Aligned with IEEE 802.3bs
- 4x50G PAM4 LAN-WDM transmitter
- 26.5625 Gbit/s Channel Electrical Serial Interface (200GAUI-8)
- 53.125 Gbit/s Channel Electrical Serial Interface (200GAUI-4)
- Duplex LC receptacles
- I2C management interface
- RoHS compliant

APPLICATIONS

- 200GBASE-LR4
- Telecom networking

DESCRIPTIONS

Opway's OPDH10 QSFP-DD transceiver modules are designed for use in 200 Gigabit Ethernet links on up to 10km of single mode fiber. They are compliant with the QSFP-DD MSA, IEEE P802.3bs. Digital diagnostic functions are available via the I2C interface, as specified by the MSA.

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Transceiver Block Diagrams

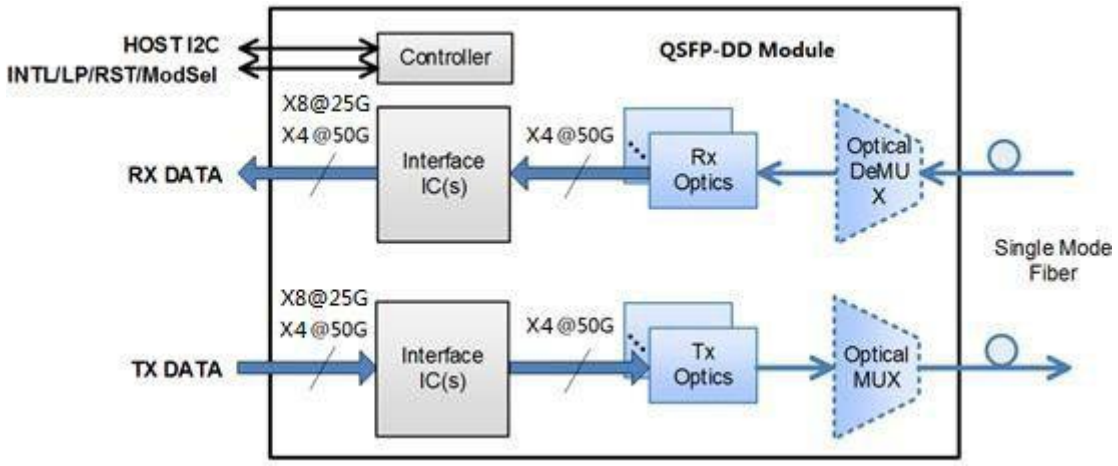

Figure 1. Transceiver Block Diagram

ModSelL:

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DDmodule.

When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. WhenMod-SelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time beforecommunicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL:

The ResetL signal shall be pulled to Vcc in the module. A low level on theResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

InitMode:

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or modulehardware control (InitMode deasserted Low). Under host soft-

ware control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

ModPrsL:

ModPrsL must be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted "Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL:

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.

Pin Descriptions

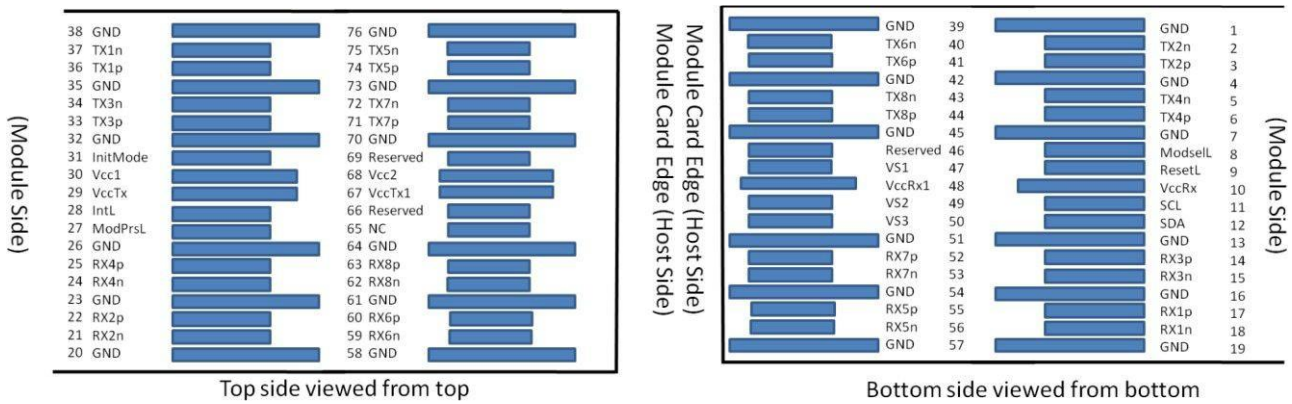

Figure 2. QSFP-DD compliant 76pin Connector

Pin	Symbol	Description	Plug Sequence	Notes
1	GND	Ground	1B	
2	Tx2n	Transmitter Inverted Data Input	3B	

3	Tx2p	Transmitter Non-Inverted Data Input	3B	
4	GND	Ground	1B	
5	Tx4n	Transmitter Inverted Data Input	3B	
6	Tx4p	Transmitter Non-Inverted Data Input	3B	
7	GND	Ground	1B	
8	ModSelL	Module Select	3B	
9	ResetL	Module Reset	3B	
10	VccRx	+3.3V Power Supply Receiver	2B	
11	SCL	2-wire serial interface clock	3B	
12	SDA	2-wire serial interface data	3B	
13	GND	Ground	1B	
14	Rx3p	Receiver Non-Inverted Data Output	3B	
15	Rx3n	Receiver Inverted Data Output	3B	
16	GND	Ground	1B	
17	Rx1p	Receiver Non-Inverted Data Output	3B	
18	Rx1n	Receiver Inverted Data Output	3B	
19	GND	Ground	1B	
20	GND	Ground	1B	
21	Rx2n	Receiver Inverted Data Output	3B	
22	Rx2p	Receiver Non-Inverted Data Output	3B	
23	GND	Ground	1B	
24	Rx4n	Receiver Inverted Data Output	3B	
25	Rx4p	Receiver Non-Inverted Data Output	3B	
26	GND	Ground	1B	
27	ModPrsL	Module Present	3B	
28	IntL	Interrupt	3B	
29	VccTx	+3.3V Power supply transmitter	2B	
30	Vcc1	+3.3V Power supply	2B	
31	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32	GND	Ground	1B	
33	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	Transmitter Inverted Data Input	3B	
35	GND	Ground	1B	
36	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	Transmitter Inverted Data Input	3B	
38	GND	Ground	1B	
39	GND	Ground	1A	
40	Tx6n	Transmitter Inverted Data Input	3A	

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41	Tx6p	Transmitter Non-Inverted Data Input	3A	
42	GND	Ground	1A	
43	Tx8n	Transmitter Inverted Data Input	3A	
44	Tx8p	Transmitter Non-Inverted Data Input	3A	
45	GND	Ground	1A	
46	Reserved	For future use	3A	
47	VS1	Module Vendor Specific 1	3A	
48	VccRx1	3.3V Power Supply	2A	
49	VS2	Module Vendor Specific 2	3A	
50	VS3	Module Vendor Specific 3	3A	
51	GND	Ground	1A	
52	Rx7p	Receiver Non-Inverted Data Output	3A	
53	Rx7n	Receiver Inverted Data Output	3A	
54	GND	Ground	1A	
55	Rx5p	Receiver Non-Inverted Data Output	3A	
56	Rx5n	Receiver Inverted Data Output	3A	
57	GND	Ground	1A	
58	GND	Ground	1A	
59	Rx6n	Receiver Inverted Data Output	3A	
60	Rx6p	Receiver Non-Inverted Data Output	3A	
61	GND	Ground	1A	
62	Rx8n	Receiver Inverted Data Output	3A	
63	Rx8p	Receiver Non-Inverted Data Output	3A	
64	GND	Ground	1A	
65	NC	No Connect	3A	
66	Reserved	For future use	3A	
67	VccTx1	3.3V Power Supply	2A	
68	Vcc2	3.3V Power Supply	2A	
69	Reserved	For Future Use	3A	
70	GND	Ground	1A	
71	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	Tx7n	Transmitter Inverted Data Input	3A	
73	GND	Ground	1A	
74	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	Tx5n	Transmitter Inverted Data Input	3A	
76	GND	Ground	1A	

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	0		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	10		85	%	1
Damage Threshold（each lane）	THd			6.3	dBm	

Notes
1. Non-condensing

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Case Temperature	Top	0		70	℃	
Supply Current	Icc			3.27	A	
Power Supply Noise	Vrip			2% 3%		DC-1MHz 1-10MHz

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation				10.8	W	
Supply Current	Icc			3.27	A	Steady state
Transmitter						
Data Rate, each lane			26.5625		Gbps	
Differential Voltage pk-pk	Vpp			900	mV	At 1 MHz
Common Mode Voltage	Vcm	-350		2850	mV	

Transition time	Trise/Tfall	9.5			ps	20%~80%
Differential impedance			100		Ω	
Eye width			0.57		UI	
Eye height			228		mV	
Receiver						
Data Rate, each lane			26.5625		Gbps	
Differential Voltage pk-pk	Vpp	900			mV	At 1 MHz
Common Mode Voltage	Vcm	-350		2850	mV	
Differential impedance			100		Ω	
Transition time	Trise/Tfall	9.5			ps	20%~80%
Eye width			0.46		UI	
Eye height A			95		mV	
Eye height B			80		mV	

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.

Optical Characteristics

200GBASE-LR4 Operation（EOL, TOP = 0 to +70℃, VCC = 3.135 to 3.465 Volts）

Parameters	Unit	min	type	max	Note
Transmitter					
Signaling Speed per Lane	Gb/s	26.5625 ± 100 ppm			
Transmit wavelengths	nm	1294.53		1296.59	
		1299.02		1301.09	
		1303.54		1305.63	
		1308.09		1310.19	
Average Launch Power, each lane	dBm	-3.4		+5.3	
Outer Optical Modulation Amplitud, each lane (OMAouter)	dBm	-0.4		+5.1	
Channel power difference	dB			4	

Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	dB			3.4	

Extinction Ratio (ER)	dB	3.5			
Side-Mode Suppression Ratio (SMSR)	dB	30			
Transmitter reflectance	dB			-26	
Receiver					
Signaling Speed per Lane	Gb/s	26.5625 ± 100 ppm			
Receive wavelengths	nm	1294.53		1296.59	
		1299.02		1301.09	
		1303.54		1305.63	
		1308.09		1310.19	
Average receiver power, each lane	dBm	-9.7		5.3	
Channel power difference	dB			4.2	
Damage threshold, each lane	dBm	6.3			
Receiver sensitivity to overload (OMAouter), each lane	dBm	-7.7		5.1	
LOS Assert	dBm	-25.7			
LOS Deassert	dBm			-11.7	
LOS Hysteresis	dB	0.5			
Receiver reflectance	dB			-26	
Stressed receiver sensitivity (OMAouter), each lane (max)）	dBm			-5.2	
Conditions of stressed receiver sensitivity test:					
Stressed eye closure for PAM4 (SECQ), lane under test	dB		3.4		
OMAouter of each aggressor lane	dBm		-1		

Note：

1. For the requirement of receiver sensitivity, the value of BER is 2e-4(before FEC) and within the average receive power, the BER is 1e-12(after FEC).

2. This value is just a reference value, not used to signal quality judgment.

3. Ieee 802.3 ba Table 88-8, Test condition refer the standard of ieee 802.3 ba Table 88-8.

EEPROM Definitions

Common Management Interface Specification Draft Rev 4.0 of QSFP-DD.

Digital Diagnostic Monitoring Functions

OPDH10 support the I2C-based Diagnostic Monitoring Interface (DMI) defined in document QSFP- DD-CMIS-rev4p0. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Performance Item	Related Bytes	Monitor Error	Notes
Module temperature	14 to 15**(Low Page)**	+/-3°C	1，2
Module voltage	16 to 17**(Low Page)**	< 3%	2
LD Bias current	170 to 177**(Page 11h)**	< 10%	2
Transmitter optical power	154 to 161**(Page 11h)**	< 3dB	2
Receiver optical power	186 to 193**(Page 11h)**	< 3dB	2

Note

1, Actual temperature test point is fixed on module case around Laser Array.
2, Full operating temperature range

Alarm and Warning Thresholds

OPDH10 support alarms function, indicating the values of the preceding basic performance are lower or higher than the thresholds.

Performance Item	Alarm Threshold (Page 02)	Low threshold	High threshold
Temp Alarm	128 to 131	-10 ℃	80 ℃
Temp Warning	132 to 135	0 ℃	70 ℃
Voltage Alarm	136 to 139	2.97 V	3.63 V
Voltage Warning	140 to 143	3.135 V	3.465 V
TX Power Alarm	176 to 179	-7.3 dBm	7.5 dBm
TX Power Warning	180 to 183	-4.3 dBm	4.5 dBm
RX Power Alarm	192 to 195	-13.6 dBm	7.5 dBm
RX Power Warning	196 to 199	-10.6 dBm	4.5 dBm

Mechanical Specifications

Opway's OPDH10 QSFP-DD transceivers are compatible with the QSFP-DD Type 2 Specifica- tion for pluggable form factor modules.

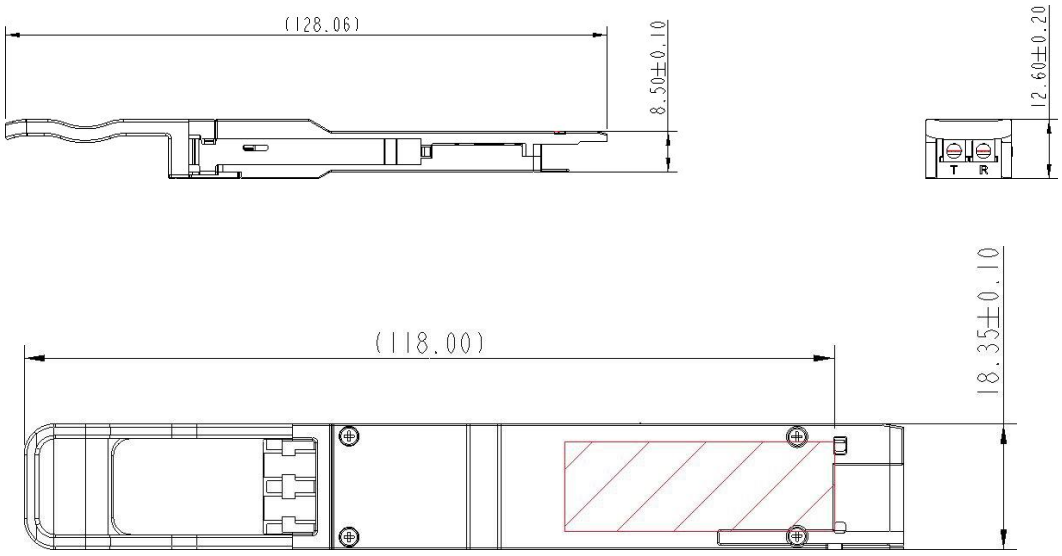

Figure 3. Mechanical Dimensions

Ordering Information

Part Number	Description
OPDH10	200GBASE-LR4 QSFP-DD, 10Km